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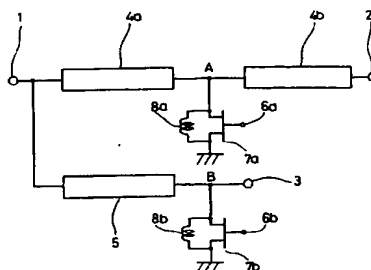
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(54) Microwave switch circuit and an antenna apparatus.

(57) A microwave switch circuit includes a first impedance conversion circuit (4a) one end of which is connected to an input/output terminal (1); a resonance circuit connected between the output of the first impedance conversion circuit (4a) and ground, in parallel connection of a field effect transistor (7) and a resonance inductor (8); and a second impedance conversion circuit (4b) connected between the output of the first impedance conversion circuit (4a) and an input terminal (2). A microwave switch circuit may be connected between an antenna side terminal (1) and a transmission wave input terminal (2) and another microwave switch circuit may be connected between the antenna side terminal (1) and a receiving wave output terminal (3). The microwave switch circuit may include the output terminal (3) and the input terminal (2) having an impedance of 50 Ω and the output end of the first impedance conversion circuit (4a) having a low impedance lower than 50 Ω and the microwave switch circuit may include one-fourth wavelength transmission lines (5) as the first and the second impedance conversion circuits (4a and 4b). Consequently, the maximum allowable value of the incident power is increased and a withstand power is increased in an antenna switch circuit.

Fig. 1



FIELD OF THE INVENTION

The present invention relates to a microwave switch circuit and an antenna apparatus, more particularly, to a switch circuit employing a resonance circuit comprising a field effect transistor (referred to as FET, hereinafter) and an inductor, and an impedance conversion circuit, and an antenna apparatus using this microwave switch circuit.

PRIOR ART

Conventionally, microwave switch circuits are each constructed by a resonance circuit comprising an FET and an inductor and a transmission line. Figure 7 shows an example of a prior art microwave switch circuit. In the figure, reference numeral 15 designates an input terminal and reference numeral 16 designates an output terminal. A transmission line 14 is provided connected between the input terminal 15 and the output terminal 16. FETs 7a, 7b are provided at the input terminal side and the output terminal side of the transmission line 14, respectively. Reference numerals 6a and 6b designate gate bias terminals of the FETs, respectively. Resonance inductors 8a and 8b are connected with the FETs 7a and 7b, respectively. A 50 Ω terminating resistor 17 is provided inserted between the resonance circuit comprising the input terminal side FET 7a and the resonance inductor 8a, and the ground. The switch circuit of this construction functions to control the transmission of the signal wave input from the input terminal 15 by turning on or off the bias to the gate bias terminals 6a and 6b of the FETs 7a and 7b.

The operation of this switch circuit will be described.

Figure 8 shows an equivalent circuit of the switch circuit of figure 7 in a case where a gate bias is applied to the gate bias terminal 6 at the both of the input side and the output side, i.e., in a state where both FETs 7a and 7b are in off states. When FETs 7 are in off states, resonance circuits are produced by the off capacitances 9 of the FETs 7 due to the depletion layers thereof and the resonance inductors 8. Then, the impedances viewed from the points C and D towards the FETs sides, i.e., the ground sides are infinite at the microwave. Then, the signal entered from the input terminal 15 is transmitted through the transmission line 14 to the output terminal 16.

On the other hand, figure 9 shows an equivalent circuit where both FETs 7 are in on states. Then, the FETs 7 are represented by the on resistances 10 which are resistances of the operating layers of the FETs 7 in on states. Then, the microwave is absorbed by the resistor 17 from the point C and is not transmitted to the output terminal 16. That is, the whole switch circuit is in off state.

Figure 10 shows an equivalent circuit of the FET 7. reference numerals 8 and 9 in the figure represent the above-described resonance inductor and off capacitance, respectively. Reference numeral 18 designates gate to drain resistance R_{gd} , reference numeral 19 designates gate to drain capacitance C_{gd} , reference numeral 20 designates gate to source capacitance C_{gs} , and reference numeral 21 designates gate to source resistance. Figure 11 shows a voltage applied between drain and source of the FET 7 when microwave enters from the input terminal 15. As can be seen from the figure, this voltage is a sinusoidal wave of an amplitude of $V_{dsRF}/2$. Then, this voltage is divided by the gate bias terminal 6. The voltage applied between the gate and drain then is represented as V_{gRF} in figure 12. Here, when a negative voltage is applied to the gate bias terminal 6 of the FET 7, the voltage V_{gRF} is shifted by $-V_{gbias}$ relative to the gate voltage vs current characteristic as shown in the figure. Therefore, the voltage V_{gRF} locally reaches the breakdown voltage V_{br} of the FET 7.

On the other hand, the allowable maximum value of power that is applicable to the FET 7 is represented by the following formula;

$$P_{max} = \frac{2 (V_g - V_{br})^2}{Z}$$

where

V_g : gate bias voltage applied to the FET 7

V_{br} : breakdown voltage of the FET 7

Z: characteristic impedance of the transmission line of a portion connected to the FET 7 (point E in figure 10).

In the microwave switch circuit having the above-described structure, the power applicable to this microwave switch circuit is regulated by the gate bias voltage V_g and the breakdown voltage V_{br} of the FET, and therefore when an excessively too large power is applied to this switch circuit, the gate voltage V_g exceeds the breakdown voltage V_{br} , thereby destroying the FET. In addition, it is neither easy to improve
 5 the breakdown voltage nor difficult to improve the withstand power of the switch.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a microwave switch circuit that improves the withstand
 10 power of the switch circuit employing the same FET as in the prior art.

It is another object of the present invention to provide an antenna apparatus using this microwave switch circuit.

Other objects and advantages of the present invention will become apparent from the detailed description given hereinafter; it should be understood, however, that the detailed description and specific
 15 embodiment are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to the those skilled in the art from this detailed description.

According to a first aspect of the present invention, a microwave switch circuit includes an impedance conversion circuit inserted between an input terminal and an FET and another impedance conversion circuit inserted between the FET and an output terminal so as to lower the impedance of a portion where the FET
 20 is connected to a transmission line.

Therefore, the impedance of the portion connected to the FET part can be lowered, resulting in an improved withstand power of a switch circuit.

According to a second aspect of the present invention, the microwave switch circuit is provided between the antenna side terminal and a transmission wave input terminal in an antenna apparatus.

25 According to a third aspect of the present invention, a pair of the microwave switch circuits is provided, one of which is provided between the antenna side terminal and a transmission wave input terminal and the other of which is provided between the antenna side terminal and the receiving wave output terminal in an antenna apparatus.

According to a fourth aspect of the present invention, a microwave switch circuit includes the output
 30 terminal and the input terminal having an impedance of $50\ \Omega$ and the output end of the first impedance conversion circuit having an output impedance lower than $50\ \Omega$.

In addition, according to a fifth aspect of the present invention, a microwave switch circuit includes one-fourth wavelength transmission lines as the first and the second impedance conversion circuits.

In this case, the maximum allowable value of the incident power can be increased and the withstand
 35 power can be increased in an antenna switch circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a microwave switch circuit according to a first embodiment of the present invention.

40 Figure 2 illustrates an equivalent circuit in a receiving state of the microwave switch circuit of the first embodiment.

Figure 3 illustrates an equivalent circuit in a transmitting state of the microwave switch circuit of the first embodiment.

45 Figure 4 illustrates simulation results at the transmitting side of the microwave switch circuit of the first embodiment.

Figure 5 illustrates simulation results at the receiving side of the microwave switch circuit of the first embodiment.

Figure 6 illustrates an example of a pattern construction of the microwave switch circuit of the first embodiment.

50 Figure 7 illustrates an equivalent circuit of a prior art microwave switch circuit.

Figure 8 illustrates an equivalent circuit of the prior art microwave switch circuit in its on state.

Figure 9 illustrates an equivalent circuit of the prior art microwave switch circuit in its off state.

Figure 10 illustrates an equivalent circuit of the FET part of the prior art microwave switch circuit.

Figure 11 illustrates a waveform of the incident wave of the prior art microwave switch circuit.

55 Figure 12 illustrates a voltage applied to the gate of the FET part of the prior art microwave switch circuit.

Figure 13 illustrates a microwave switch circuit according to a third embodiment of the present invention.

Figure 14 illustrates an example of a pattern construction of the third embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

5 Embodiment 1.

Figure 1 is a diagram illustrating a circuit of a transmitting and receiving switch in an antenna apparatus employing a microwave switch circuit according to a first embodiment of the present invention.

10 In the figure, reference numeral 1 designates an antenna side terminal, reference numeral 2 designates a transmission wave input terminal, and reference numeral 3 designates a receiving wave output terminal. A one-fourth wavelength transmission line 5 is connected to the antenna side terminal 1 at its one end and is connected to the receiving output terminal 3 at its another end. A first impedance converter 4a comprising a one-fourth wavelength line is connected to the antenna side terminal 1 at its one end and to the point A of low impedance at its another end. A second impedance converter 4b comprising a one-fourth wavelength
15 line is connected to the point A of low impedance at its one end and to the transmission wave input terminal 2 at its another end. Here, the respective characteristic impedance of the one-fourth wavelength transmission line 5 and the first and the second impedance converters 4a and 4b are that the characteristic impedance of the one-fourth wavelength transmission line 5 at the receiving side is 50 Ω , the impedance of the point A of low impedance is 12.5 Ω , and the characteristic impedances of the first and the second
20 impedance converters 4a and 4b are 25 Ω from the calculation with the both impedances.

In addition, reference numerals 6a, 6b, 7a, 7b, 8a, and 8b are gate bias terminals, FETs, and resonance inductors, respectively.

Figures 2 and 3 respectively illustrate equivalent circuits of the receiving state and the transmitting state of the above-described switch circuit. In the figures, reference numeral 9 designates a capacitance of the
25 FET at off state and reference numeral 10 designates a resistance of the FET at on state.

A description is given of the operation of the switch circuit of figure 1.

In figure 1, the characteristic impedances of the antenna side terminal 1, the transmission wave input terminal 2, and the receiving wave output terminal 3 are supposed to be Z_0 . Figure 2 shows an equivalent
30 circuit in a case where the FET at the transmitting side in figure 1 is in on state, i.e., where a gate bias is not applied to the gate of the FET, and in this case, the portion of point B in the figure is at high impedance due to the resonance by the off capacitance of FET 9 and the resonance inductor 8 while the antenna side terminal 1 is at low impedance due to the one-fourth wavelength transmission line 5. On the other hand, the part of point A in the figure is then at low impedance due to the resistance 10 of the FET in on state while it is at high impedance at the antenna side terminal 1. Therefore, the electric wave entering from the antenna
35 terminal 1 transmits to the side of point B, i.e., to the side of the receiving wave output terminal 3. Then, the FET 7b at the receiving side is at high impedance as represented by the capacitance 9 of FET in off state while the power applied to the gate does not reach the breakdown voltage V_{br} because the received electric wave is small.

Figure 3 shows an equivalent circuit when the FET at the receiving side is in on state in figure 1. The
40 impedance at point B at the receiving side then is low, and therefore, the impedance viewed from the antenna side terminal 1 is high and the transmission path of the electric wave then is the side of point A, i.e., the side of the transmission wave input terminal 2. Then, the FET 7a at the side of point A is resonating, and the FET itself is at high impedance as represented by the off state capacitance 9 while the impedance of the transmission line at the connecting portion A with the FET is at low impedance less than
45 the impedance 50 Ω of the input and output terminals 2 and 3 due to the impedance converters 4a and 4b which lead to raising the maximum allowable value of the incident power, thereby preventing the destruction of the FET 7a at the side of point A. For example, when supposed the impedance Z_0 of the input terminal 2 is 50 Ω , the gate bias voltage V_{gbias} -5V, and the breakdown voltage V_{br} -7V, and the impedance at point A 12.5 Ω by that the impedance converters 4a and 4b are constituted by one-fourth wavelength transmission
50 lines of characteristic impedance of $\sqrt{(50 \times 12.5)} = 25 \Omega$, the maximum allowable value of the incident power P_{max} becomes as represented by the following formula;

$$55 \quad P_{max} = \frac{2}{12.5} \{-5 - (-7)\}^2 = 0.64 \text{ W.}$$

Meanwhile, when the prior art one-fourth wavelength transmission line of $50\ \Omega$ is employed in place of the impedance converter 4, the impedance of the transmission line at point A becomes $50\ \Omega$ and the maximum allowable value of the incident power P_{\max} is represented by the following formula;

$$P_{\max} = \frac{2}{50} \{-5 - (-7)\}^2 = 0.16\ \text{W}.$$

This means that it is possible to improve the withstand power of the switch circuit to four times as that of the prior art switch by the construction of this first embodiment.

Figure 4 and 5 show simulation results of the switch circuit of this embodiment of figure 1 when this circuit is employed for switching small signals.

In the figure, it is supposed that the antenna side terminal 1 is port 1, the transmission wave input terminal 2 is port 2, and the receiving wave terminal side 3 is port 3. This simulation is carried out, supposing the frequency band for transmission is 14 GHz band and that for receiving is 12 GHz. Figure 4 shows the simulation results and it can be seen that the transmission loss (S21) of the transmission wave from the transmission wave input terminal 2 to antenna side terminal 1 is 0.59 dB, the return loss (S21, S22) between the input and output is below 25 dB, and the isolation (S31) between the receiving wave output terminal 3 and the antenna side terminal 1 is -33 dB, including sufficient isolation.

Figure 5 shows simulation results at the receiving. It is supposed that the transmission loss (S31) from the antenna side terminal 1 to the receiving wave output terminal 3 is 0.80 dB, the between input and output return loss (S11, S33) are below -22dB, and the isolation (S21) between the antenna side terminal 1 and the transmission wave input terminal 2 is secured to be -28 dB, and this circuit construction functions sufficiently as a microwave switch circuit. Here, these simulation results are values when the transmission frequency is 14 GHz and the receiving frequency is 12 GHz.

Figure 6 shows an example of a pattern construction realizing the circuit of this embodiment. In the figure, the same reference numerals as those shown in figure 1 designate the same or corresponding portions. Reference numeral 1 designates an antenna side terminal, reference numeral 2 designates a transmission wave signal input terminal, and reference numeral 3 designates a receiving wave signal output terminal. Reference numeral 4 designates an impedance converter of one-fourth wavelength, reference numeral 5 designates a one-fourth wavelength transmission line having a characteristic impedance of Z_0 , reference numerals 7a and 7b designate FETs, and reference numerals 8a and 8b designate resonance inductors. Further, reference numeral 11a, 11b, and 11c designate grounding via-holes, reference numeral 12a and 12b designate MIM capacitors for gate-biasing provided between the gate bias terminals 6a and 6b and the FETs 7a and 7b, and reference numerals 13a and 13b designate resistors for gate-biasing.

Embodiment 2.

While in the first embodiment a transmission and receiving switch circuit is described, the present invention can be constituted as a single pole single throw switch (generally called as an "SPST" switch), i.e., a switch circuit provided only between the antenna side terminal and the transmission wave input terminal, which is also obtained by removing the circuit at receiving side from the circuit of the first embodiment. This second embodiment of the present invention can also exhibit the same effect as that of the first embodiment, i.e., the effect of improving the withstand power of the switch.

Embodiment 3.

While in the first embodiment the impedance converters 4a and 4b are provided, when there is a possibility that a power relatively equal to that of the transmission enters into the receiving state, the impedance converters 4c and 4d of the same construction as that of the transmission side can be provided also at the receiving side, i.e., the side of the receiving wave output terminal 3 as shown in figure 13, with the same effect as that of the first embodiment.

Embodiment 4.

In addition, because the transmission lines 4a and 4b in the first embodiment are of large sizes due to their low impedances, these transmission lines may be produced of coplanar lines as shown in figure 14. In the figure, reference numeral 30 designates a grounding conductor constituting a coplanar line. In this fourth embodiment of such construction, the circuit is minimized.

Claims

1. A microwave switch circuit comprising:
 - a first impedance conversion circuit (4a) one end of which is connected to an input terminal (2);
 - a resonance circuit connected between the output of said first impedance conversion circuit (4a) and ground, comprising a parallel connection of a field effect transistor (7) and a resonance inductor (8); and
 - a second impedance conversion circuit (4b) connected between the output of said first impedance conversion circuit (4a) and an output terminal (3).
2. An antenna apparatus including a microwave switch circuit comprising a first impedance conversion circuit (4a) one end of which is connected to an input terminal(2), a resonance circuit connected between the output of said first impedance conversion circuit (4a) and ground, comprising a parallel connection of a field effect transistor (7) and a resonance inductor (8), and a second impedance conversion circuit (4b) connected between the output of said first impedance conversion circuit (4a) and an output terminal (3), wherein said microwave switch circuit is connected between an antenna side terminal (1) and a transmission wave input terminal (2).
3. An antenna apparatus including a microwave switch circuit comprising a first impedance conversion circuit (4a) one end of which is connected to an input terminal (2), a resonance circuit connected between the output of said first impedance conversion circuit (4a) and ground, comprising a parallel connection of a field effect transistor (7) and a resonance inductor (8), and a second impedance conversion circuit (4b) connected between the output of said first impedance conversion circuit (4a) and an output terminal (3), wherein a pair of said microwave switch circuits is provided, one of which is connected between an antenna side terminal (1) and a transmission wave input terminal (2) and the other of which is connected between said antenna side terminal (1) and a receiving wave output terminal (3).
4. The antenna apparatus of claims 2 and 3, wherein said microwave switch circuit comprises said input terminal (2) and said output terminal (3) having an impedance of 50 Ω and the output of said first impedance conversion circuit (4a) having a low impedance less than 50 Ω .
5. The antenna apparatus of claims 2 to 4, wherein said microwave switch circuit comprises said first and said second impedance conversion circuits (4a and 4b) each comprising a one-fourth wavelength transmission line (5).
6. The antenna apparatus of claims 2 to 4, wherein said microwave switch circuit comprises said first and said second impedance conversion circuits (4a and 4b) each comprising a coplanar line.

Fig. 1

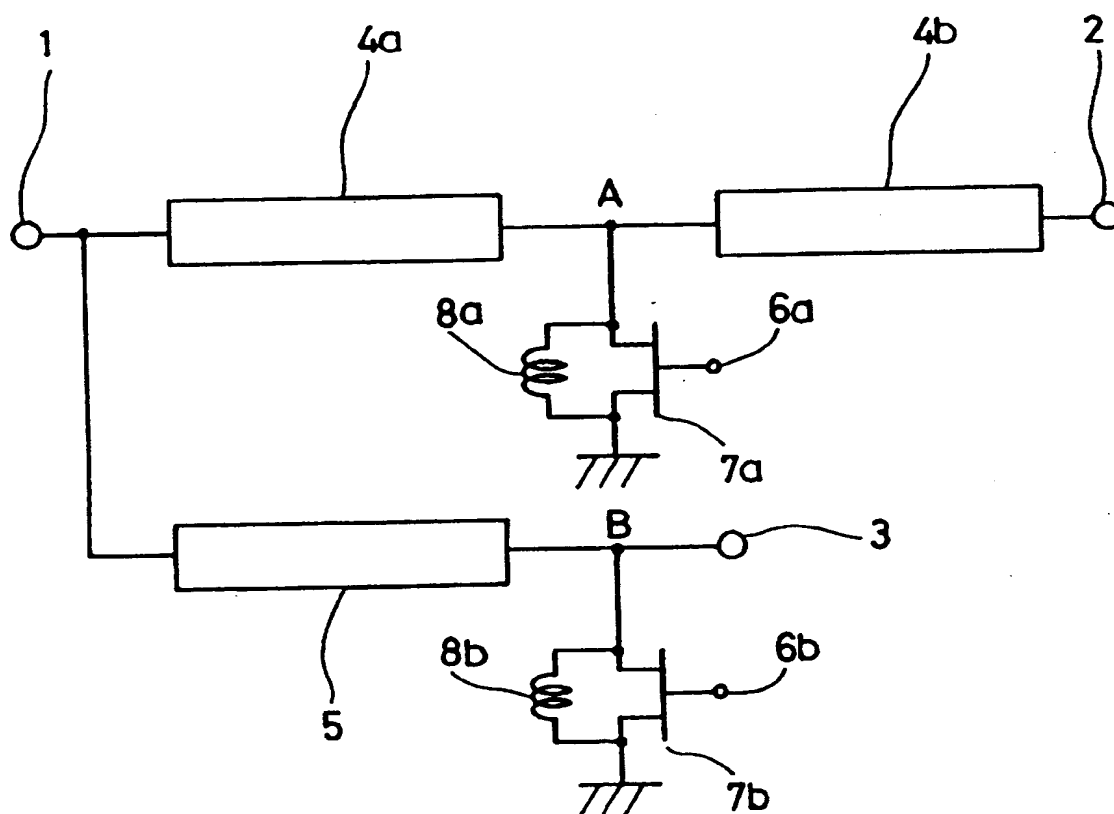


Fig. 2

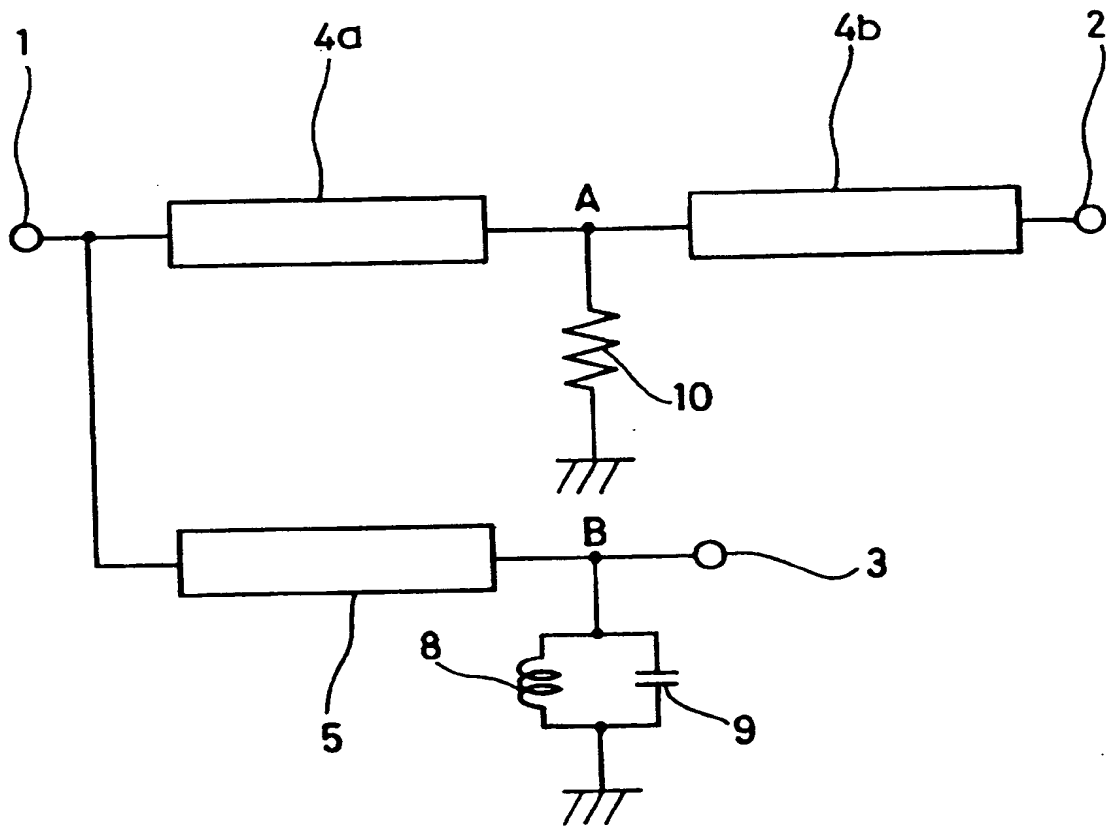


Fig. 3

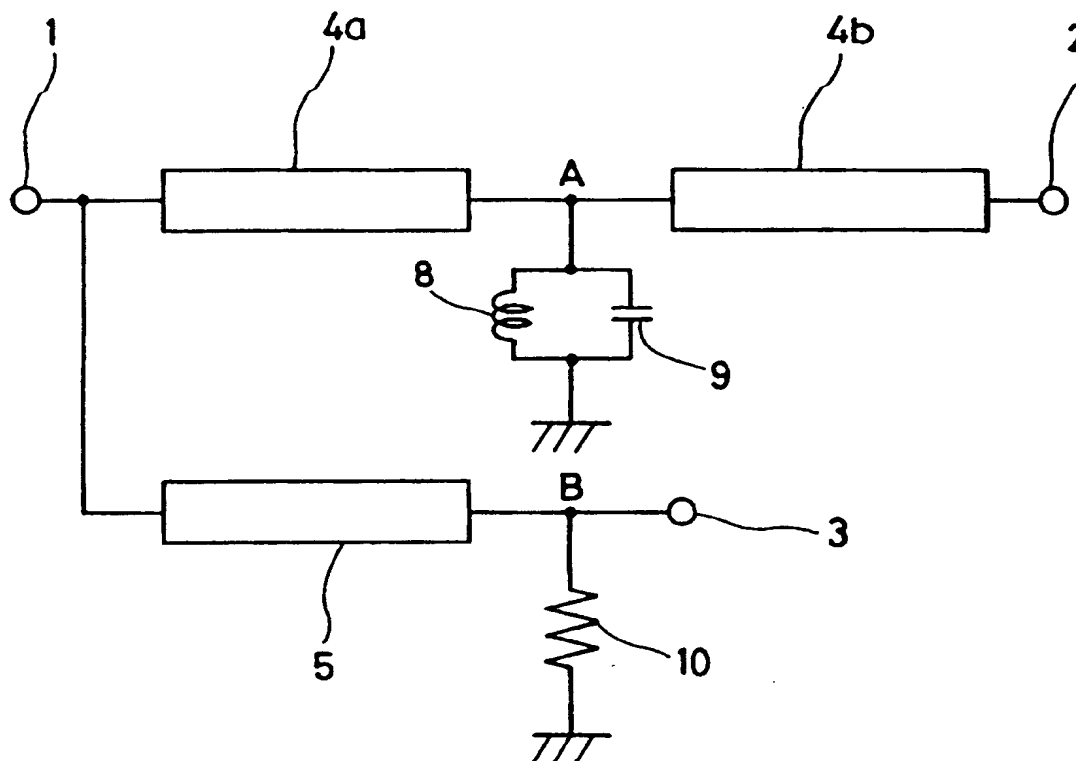


Fig. 4

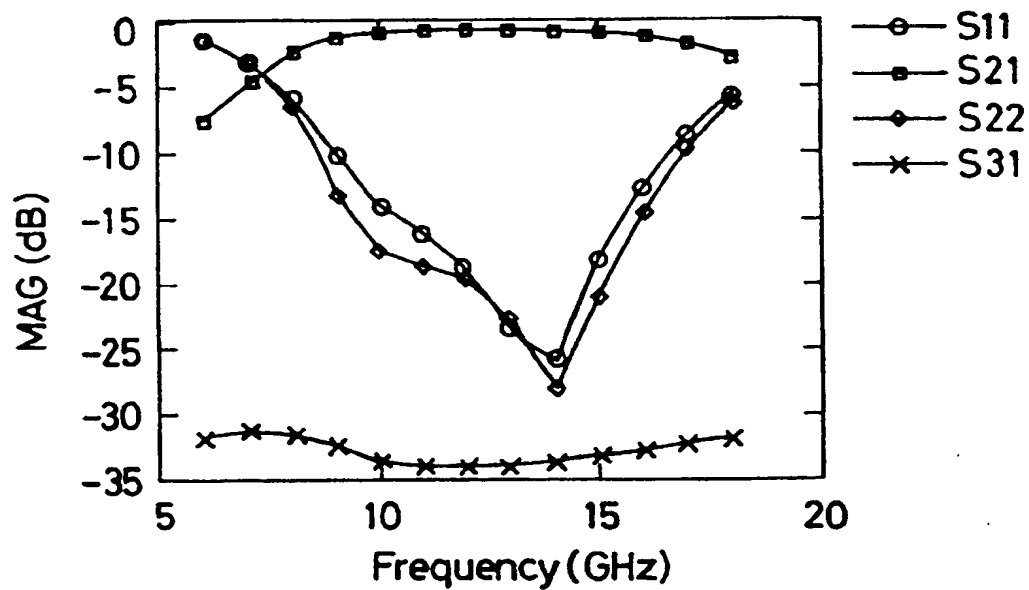


Fig. 5

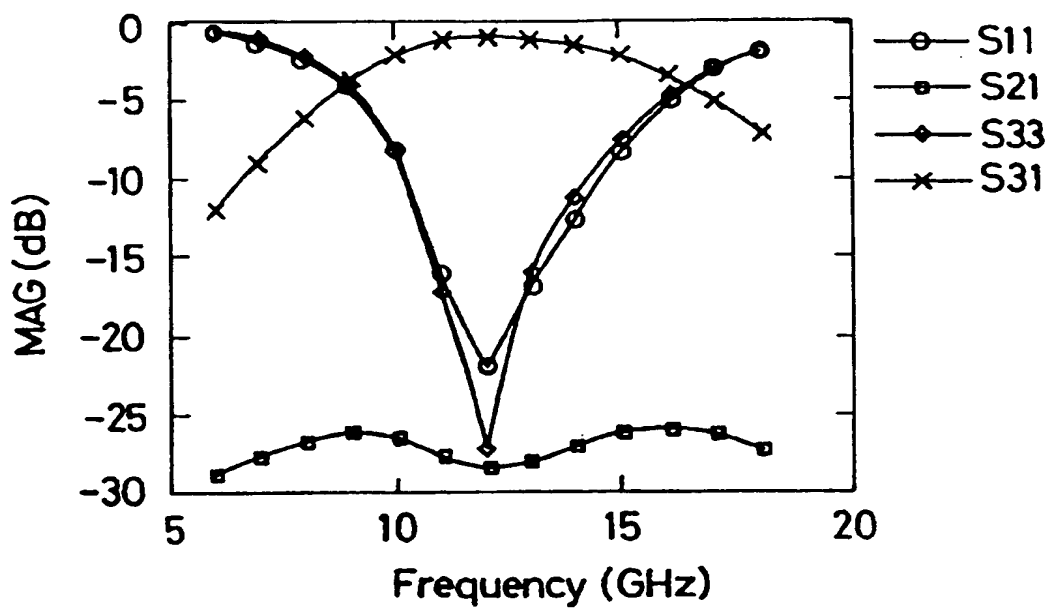


Fig. 6

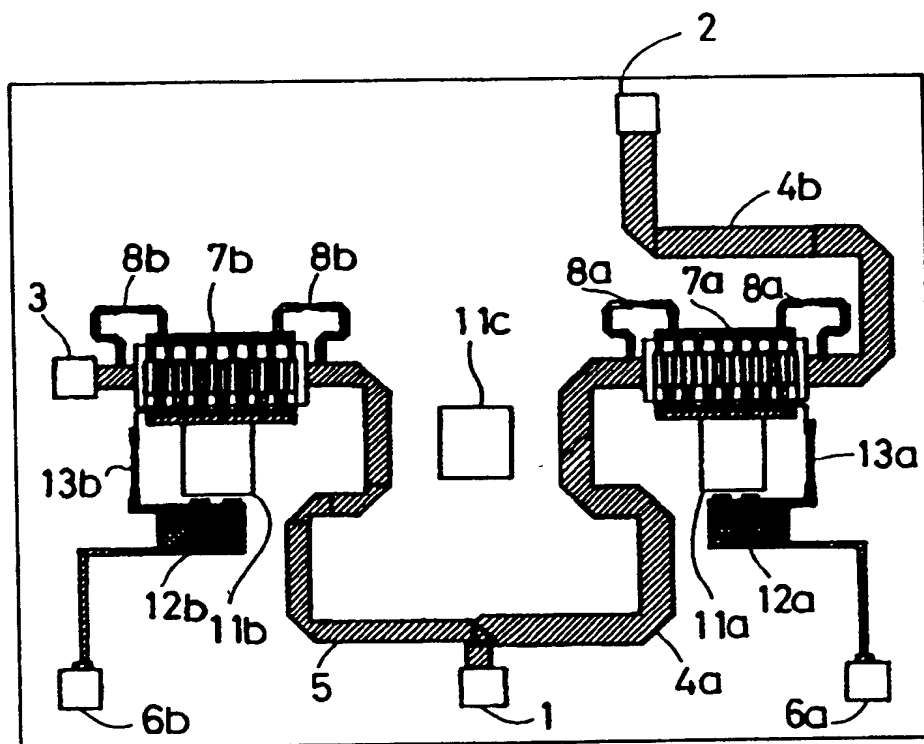


Fig. 7 (Prior Art)

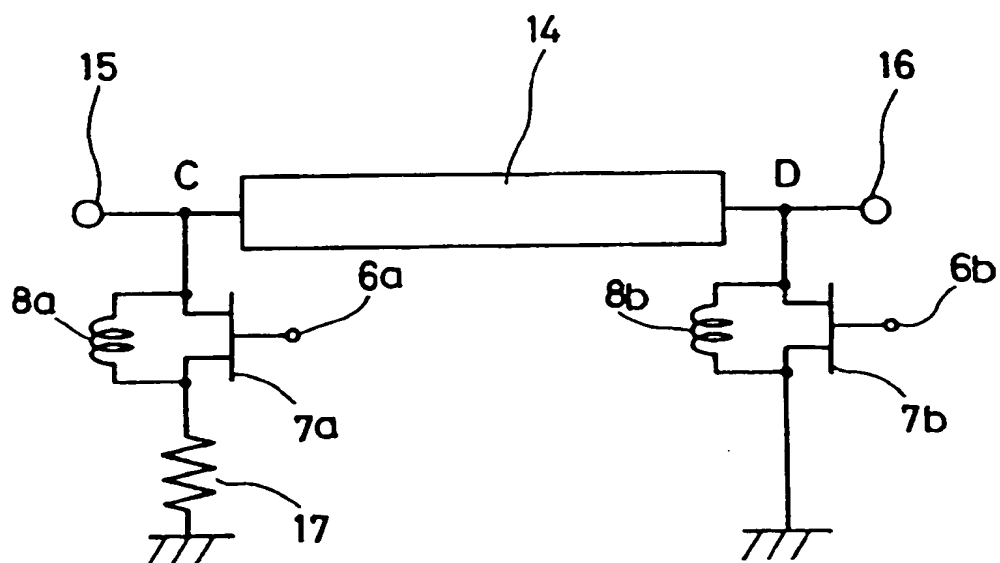


Fig. 8 (Prior Art)

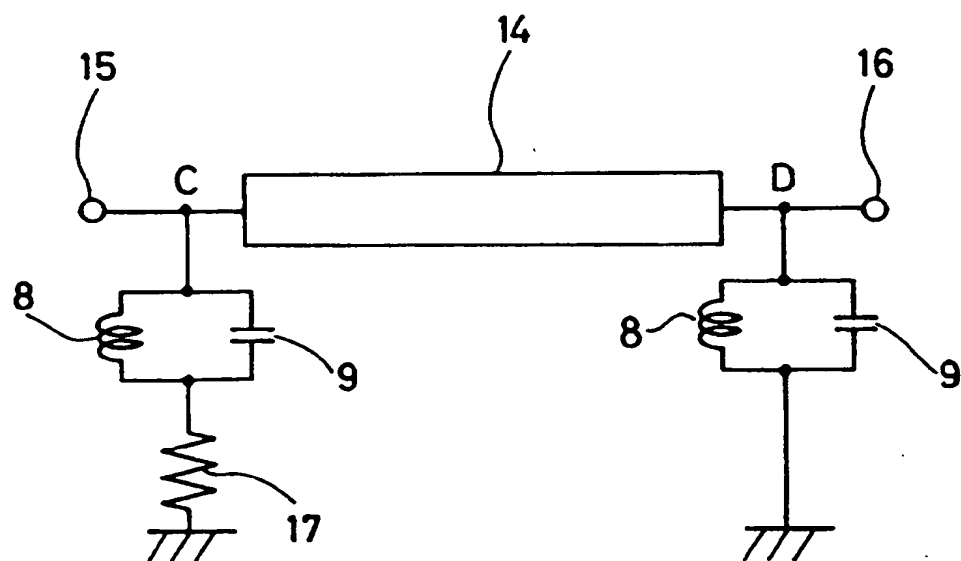


Fig.9 (Prior Art)

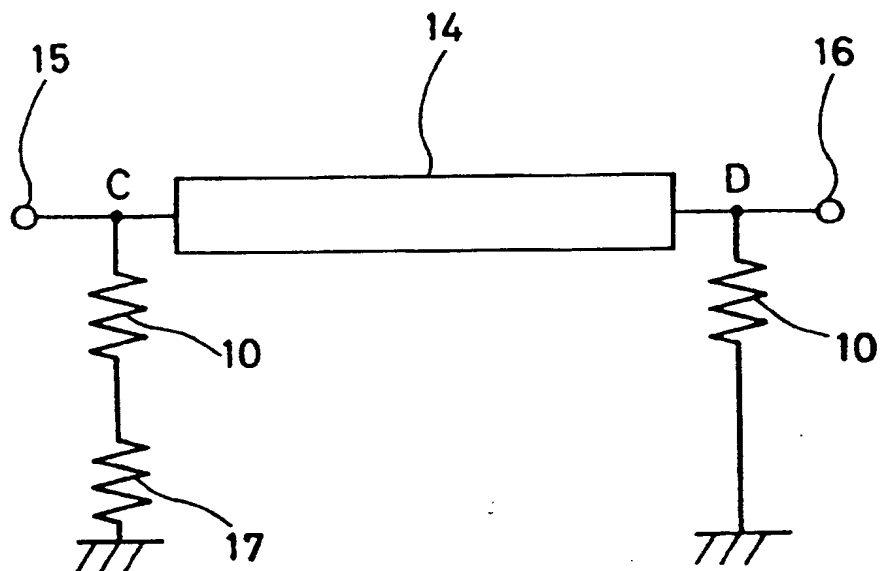


Fig.10 (Prior Art)

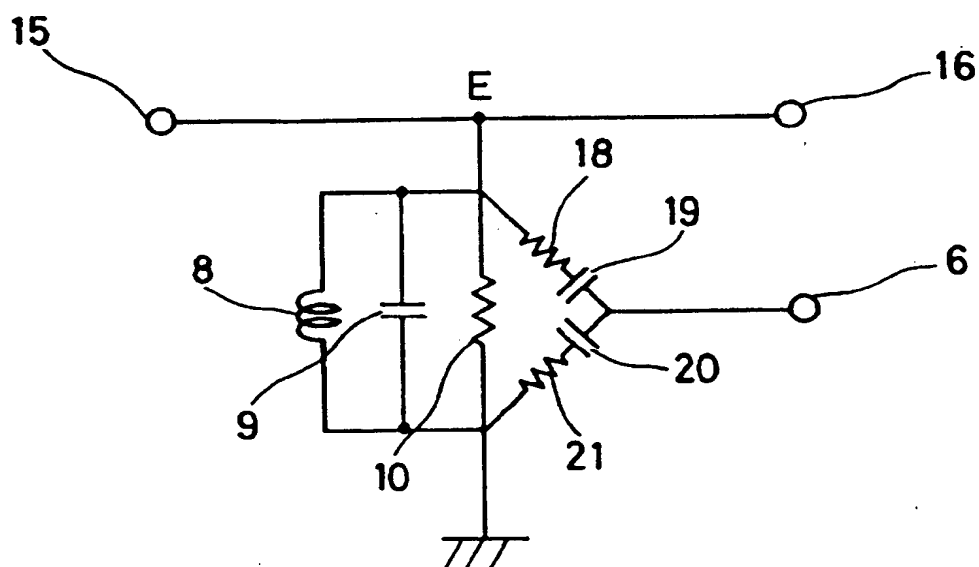


Fig. 11 (Prior Art)

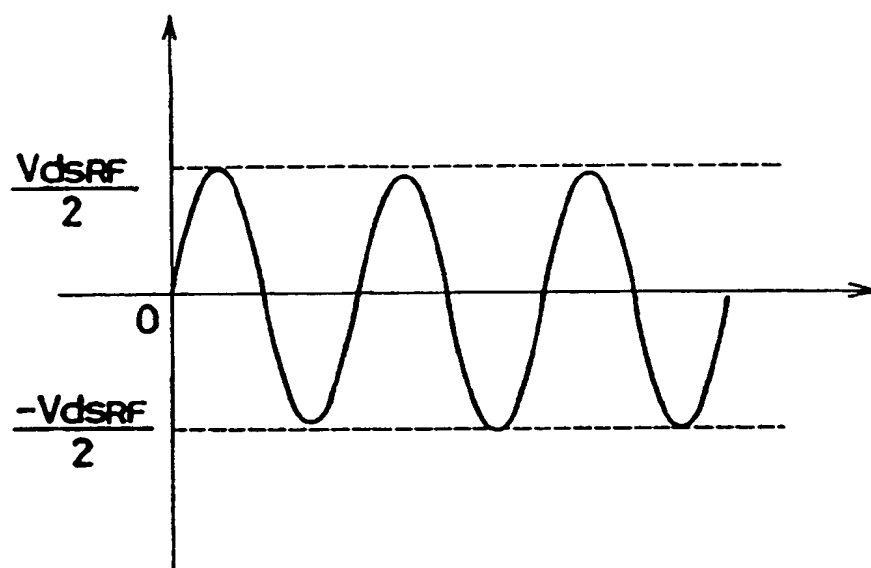


Fig. 12 (Prior Art)

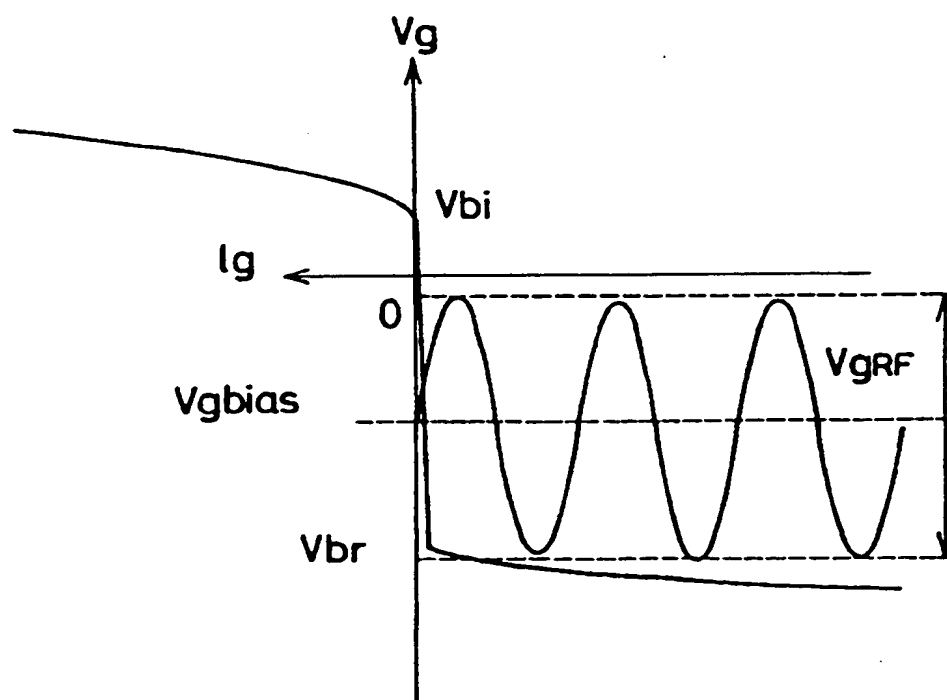


Fig. 13

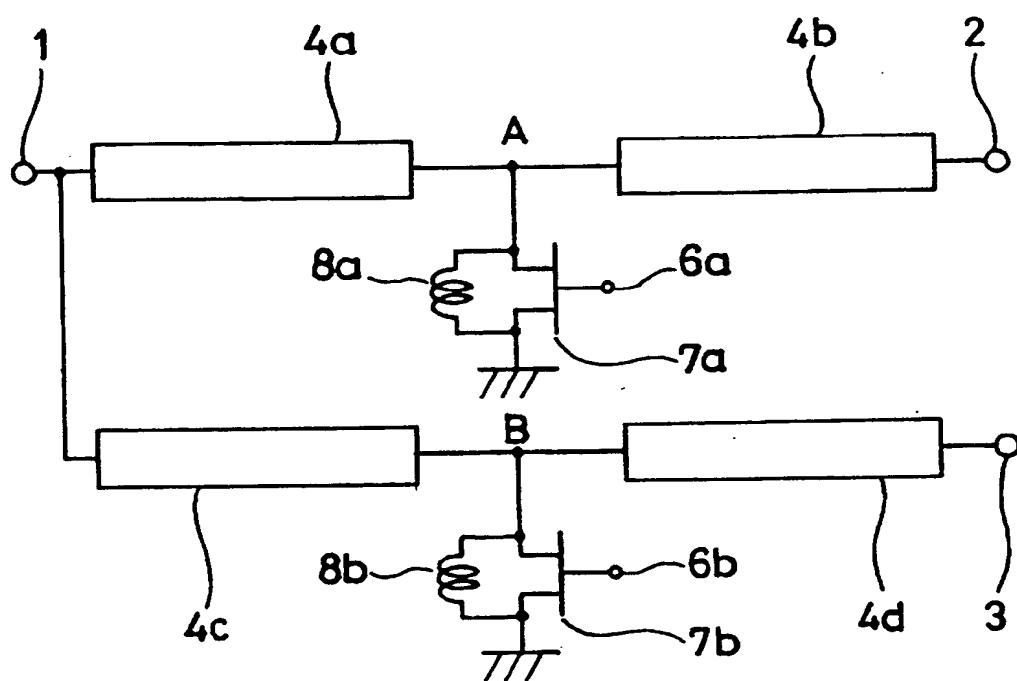
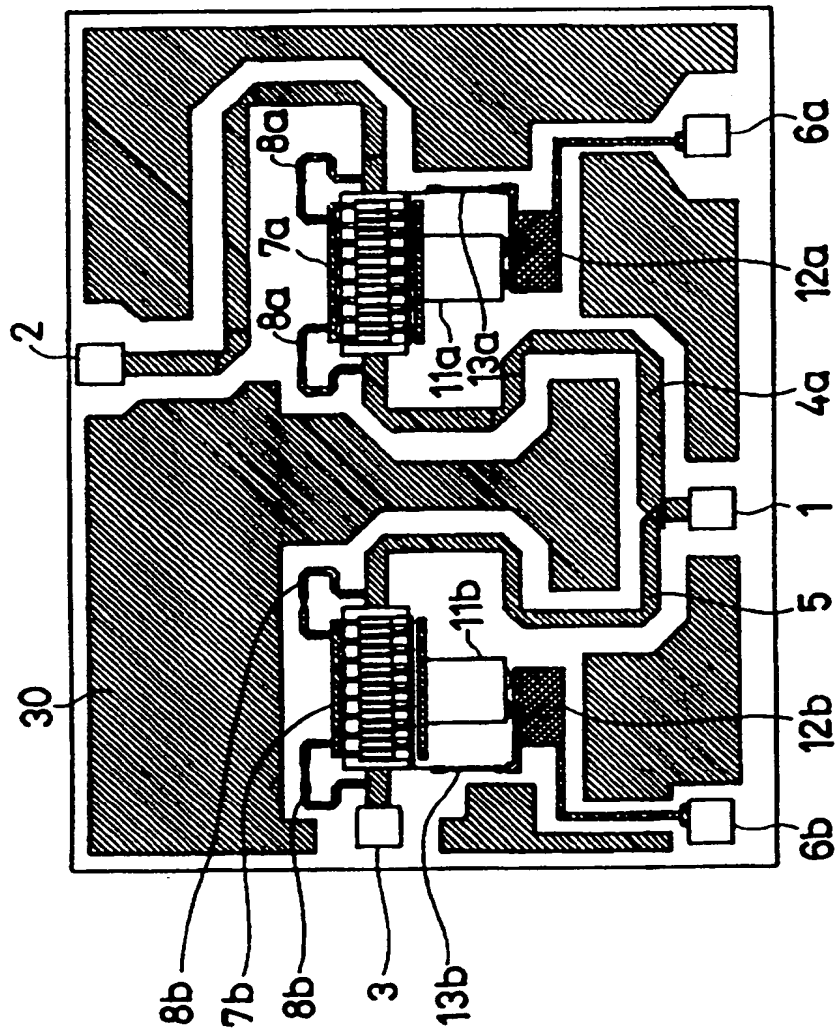


Fig. 14





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EUROPEAN SEARCH REPORT

Application Number
EP 94 10 0994

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
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A	FR-A-2 607 643 (MITSUBISHI DENKI KABUSHIKI KAISHA) * page 13, line 36 - page 16, line 30; figures 5A-6 *	1-3	
A	IEEE MTT, INTERNATIONAL MICROWAVE SYMPOSIUM DIGEST, VOL. 1, MAY 25-27, 1988, MARRIOTT MARQUIS HOTEL, JACOB JAVITS CONVENTION CENTER, NEW YORK, US pages 371 - 374 'A Monolithic Reduced-Size Ku-Band SPDT FET Switch' * Section: 'Monolithic Circuit Design'; figure 4 *	1,2	TECHNICAL FIELDS SEARCHED (Int.Cl.5) H01P H03K H04B
A	EP-A-0 409 374 (MITSUBISHI DENKI KABUSHIKI KAISHA) * figure 1 *	1	
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 24 May 1994	Examiner Arendt, M
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons * : member of the same patent family, corresponding document			

EPO FORM 1503 (01.82) (P04C01)



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EUROPEAN SEARCH REPORT

Application Number
EP 94 10 0994

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
P,A	PATENT ABSTRACTS OF JAPAN vol. 17, no. 359 (E-1395) 7 July 1993 & JP-A-05 055 803 (MITSUBISHI ELECTRIC CORP) 5 March 1993 * abstract *	1	
A	ELECTRONIC ENGINEERING, vol.56, no.695, November 1984, SOUTHEND-ON-SEA, ESSEX, GB pages 141 - 144 149 R. S. PENGELLY ET AL.: 'Transmit / receive module using GaAs ICs' * Section: 'Power switching'; figure 5 *	1-3	
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The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 24 May 1994	Examiner Arendt, M
CATEGORY F CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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